REMARKS

No claims have been amended, canceled, or added. Thus, no listing of claims is required nor provided. Claims 1-69 are pending.

Claims 65-66 and 69 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Houg (U.S. Patent No. 6,322,596). Claims 67-68 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Houg. Claims 1-35, 37-46, and 48-643 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Blackmon (U.S. Patent No. 6,513,091) in view of Houg. Claims 36 and 47 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Blackmon in view of Houg. Claims 65-69 stand rejected as being unpatentable over Blackmon.

Each of the independent claims recite a link bus having a status line, and a direct connection between a link bus hub and a link bus device. More specifically:

Claims 1 and 18 recite, *inter alia,* "A method of transferring data in a processor based system, the system comprising a hub device ... said hub device being directly connected to a first device by a link bus, the link bus having a status line, said method comprising the steps of: issuing, from one of the first device and the hub device, a data transfer request on the link bus; obtaining a status of the request by observing the status line during a first predetermined window of time...."

Claim 20 recites, *inter alia,* "A method of receiving data in a processor based system, the system comprising a hub device ... said hub device being directly connected to a first device by a link bus, the link bus having a status line, said method comprising the steps of: detecting, at one of the first device and the hub device, a data transfer request on the link bus; ... driving the status on the status line during a first predetermined window of time, wherein the status is selected from the group

consisting of an accept status indicating that the transfer can be initiated and a retry status indicating that the transfer should be retried at a subsequent period of time...."

Claim 30 recites, *inter alia*, "A method of transferring data in a processor based system, the system comprising a hub device ... said hub device being directly connected to a first device by a link bus, the link bus having a status line, said method comprising the steps of: issuing, from one of the first device and the hub device, a data transfer request on the link bus; ...:. obtaining the status of the transfer by observing the status line during the first predetermined window of time...."

Claim 37 recites, *inter alia*, "A processor system comprising: ... a link bus directly connected between said link hub and said satellite device, said link bus comprising a status line and a first bus, ..."

Claim 56 recites, *inter alia*, "A processor system comprising: ... a link bus directly connected between said link hub and said satellite device, said link bus comprising a status line and a first bus, ..."

Claim 65 recites, *inter alia*, "A processor system comprising: ... a link bus directly connected between said link hub and said satellite device, said link bus comprising a status line and a first bus, ..."

Houg is discloses a method and apparatus for obtaining status information. Referring to Fig. 5, the Office Action alleges that Houg discloses system 500 including a processor 502, a link hub 506, a satellite device 400, and a link bus 504. This conclusion is in error. As plainly evident in Fig. 5, reference numeral 506 is associated with a bridge circuit for bridging between a processor bus (coupling to processor 502), a memory bus (coupling to RAM 508), a AGP port (coupling to AGP device 510), and a PCI bus 504 (coupling to PCI devices, including devices 512 and target device 400). The

PCI bus cannot be a link bus because it is not a point-to-point bus. Simply put, Houg fails to disclose or suggest a link bus or a link bus hub.

Blackmon is directed to a data routing method and apparatus in a system comprising a link bus 36, a switch 34, and a network of status response signals 37, 42, 44. Referring to, for example, Fig. 1, Blackmon discloses a system in which bus devices 32A-32D, referred to collectively as 32 are coupled to a bus 36. The bus is a plurality of point-to-point connections 36A-36D (referred to collectively as 36), and is used to directly couple and permit communication from each one of the bus devices 32 with a switch 34. Each one of the plurality of links 36 is comprised of a data bus 40 and an address bus 38.

Blackmon also discloses a status network of status lines 37A-37D (referred collectively to as 37). Each one of the status lines 37 is coupled to a response combining logic 42. The response combining logic 42 is coupled via link 44 to the switch 34.

The Office Action alleges that Blackmon discloses a link bus system having link bus with a status line, where bus devices are directly coupled via the link bus to the hub device. As noted in the previous amendment, this conclusion is erroneous. Reconsideration is respectfully requested.

Blackmon specifically states that the "plurality of point-to-point connections 36 collectively form a system bus for the switch based topology." Column 3, lines 2-4. Blackmon further states "[a] response combining logic module 42 is coupled to each bus device 32 via address status response signals 37A, 37B, 37C, 37D, hereinafter referred to collectively as 37. Address status response signal 37 carry a signal response generated by each of the bus devices 32 in response to an issue command on the system bus." Column 3, lines 4-9. Blackmon therefore clearly describes the bus as being comprised

only of the plurality of point-to-point connections 36, and further independently describes the network of status response signals 37.

Further, with respect to the status signals, Blackmon discloses:

> The AStatOut signal is driven from each of the plurality of bus devices 32 to response combining logic module 42 where the signals are combined and redriven back to bus devices 32 via the AStatIn signal (as described in greater detail in FIG. 3.). When AStatOut signals are combined by response combining logic module 42, the highest priority signal value is determined, and that highest priority signal value is returned to the plurality of bus devices 32 via the AStatIn signal.
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> Column 4, lines 14-23.

The reason Blackmon uses a separate network of status signals and the response combining logic module 42 is to provide an alternative for requiring the use of address range registers in the switch for a link bus. See column 1, lines 22-66. Blackmon's solution is the addition of a separate status network. Accordingly, the system bus of Blackmon cannot be fairly stated to teach or suggest a link bus having a status line. Indeed, by adding a separate status network in a system where the link bus does not include a status line, Blackmon even teaches against the use of a status line within a link bus. Further, as noted above, the status lines of Blackmon do not directly link any bus device 32 with the switch 34 (i.e., "hub").

Accordingly, Houg and Blackmon, whether taken individually or in combination, does not disclose or suggest the above quoted portions of the independent claims. Independent claims 1, 18, 20, 30, 37, 56, and 65 are believed to be allowable over the prior art of record. The depending claims (i.e., claims 2-17, 19, 21-29,

31-36, 38-55, 57-64, and 66-69) are also believed to be allowable for at least the same reasons as the independent claims.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

Dated: August 18, 2004

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